REMARKS

In the last Office Action, claims 15-16 were rejected under 35 U.S.C. §102(b) as being anticipated by Wen-Shiung Lour and Chung-Cheng Chang in Solid States Electronics, vol. 39, issue 9, pp. 1295-1298 (1986) ("Wen"). The Examiner contends that Wen discloses each and every element of the photodiode recited in claims 15-16. Claims 1-7[1] were rejected under 35 U.S.C. §103(a) as being unpatentable over Wen in view of applicant's prior art disclosure in Figs. 2 and 3 ("APD"). The Examiner contends that the subject matter of claims 1-7 is taught by the combined teachings of Wen and APD. Claim 2 was rejected under 35 U.S.C. §103(a) as being unpatentable over Wen in view of APD and further in view of Chang Song Yin (IEEE Electron Device Letters, Volume 12, No. 8, pp. 442-443 (1991). The Examiner contends that the subject matter of claim 2 is taught by the combined teachings of Wen, APD and Chang Song Yin.

[1] While the Examiner included claim 2 in this ground of rejection, it is clear from pages 4-5 and 10-11 of the final Office Action that the Examiner has withdrawn the rejection of claim 2 under 35 U.S.C. §103(a) as being unpatentable over Wen in view of APD and has rejected claim 2 under 35 U.S.C. §103(a) as being unpatentable over Wen in view of APD and further in view of Chang Son Yin.

Applicant respectfully traverses the prior art rejections of claims 1-7 and 15-16 and requests reconsideration of his application in light of the following discussion.

Brief Summary of the Invention

The present invention is directed to a short-wavelength photodiode of enhanced sensitivity with low leak current.

As described in the specification (pgs. 1-3), the detection of light sensitivity in a short wavelength region by conventional photodiodes is inferior. Furthermore, the conventional photodiodes are associated with high leak current.

The present invention overcomes the drawbacks of the conventional art. Fig. 1 shows a photodiode according to the present invention embodied in independent claim 1.
The photodiode comprises an optical detection portion for detecting an optical signal and outputting a photoelectric conversion signal. The optical detection portion has a semiconductor substrate 1 of a first conductive type and semiconductor layers 2a, 2b of a second conductive type formed in spaced-apart relation in a surface of the semiconductor substrate. A depletion layer 3 is formed in the semiconductor substrate 1 by application of a reverse bias to the photodiode

so as to surround the semiconductor layers 2a, 2b. An etched surface portion (denoted by X in the copy of Fig. 1 submitted herewith as Exhibit A) of the depletion layer 3 is disposed between the semiconductor layers 2a, 2b so that an interface level region of the surface of the semiconductor substrate 1 does not exist between the semiconductor layers 2a, 2b.

By the foregoing photodiode construction, the present invention provides a short-wavelength photodiode of enhanced sensitivity and with low leak current. By etching the surface portion of the depletion layer which is disposed between the semiconductor layers so that the interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers, leak current is controlled without greatly influencing the photo sensitivity of the photodiode.

The prior art of record does not disclose or suggest the subject matter recited in independent claims 1 and 15 and dependent claims 2-7 and 16.

Traversal of Prior Art Rejections

Rejection Under 35 U.S.C. §102(b)

Claims 15-16 were rejected under 35 U.S.C. §102(b) as being anticipated by Wen. Applicant respectfully traverses this rejection and submits that claims 15-16 recite subject matter which is not disclosed or described by Wen.

Independent claim 15 is directed to a photodiode and requires an optical detection portion for detecting an optical signal and outputting a photoelectric conversion signal, the optical detection portion having a semiconductor substrate of a first conductive type and a plurality of semiconductor layers of a second conductive type disposed in spaced-apart relation in a surface of the semiconductor substrate so that an interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers. No corresponding structural combination is disclosed or suggested by the prior art of record.

Independent claim 15 recites features which are not disclosed or described by Wen. In this regard, the Examiner's attention is respectfully invited to Ex parte Levy, 17 USPQ2d 1461, 1462 (BPAI 1990), wherein the Board stated:

> The factual determination of anticipation requires the disclosure in a single reference of every element of the claimed invention. In re Spada, 15 USPQ2d 1655 (Fed. Cir. 1990); In re Bond, 15 USPQ2d 1566 (Fed. Cir. 1990) (other citations omitted). Moreover, it is incumbent upon the examiner to identify wherein each and every facet of the claimed invention is disclosed in the applied reference. Lindemann Maschinenfabrik GmbH v. American Hoist and Derrick, 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984).

Moreover, as stated by the Court of Appeals for the Federal Circuit in the case of In re Spada, 15 USPQ2d 1655, 1657 (CAFC, 1990):

> Rejection for anticipation or lack of novelty requires, as the first step in the inquiry, that all the elements of the claimed invention be described in a single reference. Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir.), cert. denied.

Similarly, as stated earlier by the Court of Customs and Patent Appeals in the case of In re Marshall, 198 USPQ 344, 346 (CCPA, 1978):

> Rejections under 35 USC 102 are proper only when the claimed subject matter is identically disclosed or described in the prior art. In re Arkely, 59 CCPA 804, 807, 455 F.2d 586, 587, 172 USPQ 524, 526 (1972). In other words, to constitute an anticipation, all material elements recited in a claim must be found in one unit of prior art. Soundscriber Corp. v. United States, 360 F.2d 954, 960, 148 USPQ 298, 301 (Ct.cl. 1966).

Wen does not describe or disclose the subject matter of independent claim 15 and thus does not anticipate this claims.

Wen discloses a PIN photodiode. With reference to Fig. 1 of Wen which has been reproduced herewith as Exhibit B, the PIN photodiode has a P-Si substrate, an n-type ZnSe layer formed on the P-Si substrate, and two n^+ layers spaced-apart

from one another and disposed on the n-type ZnSe layer. A depletion layer is formed in the n-type ZnSe layer above the P-Si substrate.

In contrast, independent claim 15 requires an optical detection portion having (1) a semiconductor substrate of a first conductive type and (2) a plurality of semiconductor layers of a second conductive type disposed in spaced-apart relation in a surface of the semiconductor substrate (3) so that an interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers. As further discussed below, each of the foregoing limitations (1)-(3) recited in claim 15 is not identically disclosed or described in Wen.

With respect to limitation (1), the Examiner contends that the P-Si substrate and the i-ZnSe absorption layer in Wen together constitute and correspond to the semiconductor substrate of independent claim 15 (Final Office Action, paragraph bridging pages 5-6). Applicant respectfully disagrees with the Examiner's contention and with the Examiner's interpretation of Wen in the rejection of claim 15.

Applicant respectfully submits that one of ordinary skill in the art would recognize that only the P-Si substrate in Wen corresponds to the semiconductor substrate recited in independent claim 15. As described in parts 1-2 of Wen, the

absorption layer i-ZnSe in Wen is a heteroepitaxial ZnSe thin film formed on the P-Si substrate by vapor phase epitaxy. After finishing the epitaxial growth, the n^+ -ZnSe layer was achieved by driving evaporated In metal into the ZnSe layer. A P-N junction is thus formed at an interface between the P-Si substrate and the i-ZnSe layer in Wen. Accordingly, contrary to the Examiner's contention, it is evident from the disclosure in Wen that the i-ZnSe layer is a separate layer which cannot be reasonably interpreted as forming a semiconductor substrate together with the P-Si substrate. Stated otherwise, only the P-Si substrate in Wen can be reasonably interpreted as the semiconductor substrate recited in independent claim 15.

With respect to limitation (2) in independent claim 15, the Examiner contends that the pair of n^+ layers in Wen correspond to the plurality of semiconductor layers of a second conductivity type disposed in spaced-apart relation in a surface of the semiconductor substrate recited in independent claim 15. Applicant respectfully disagrees with the Examiner's contention and with the Examiner's interpretation of Wen.

Applicant respectfully submits that only the i-ZnSe layer in Wen can be reasonably interpreted as corresponding to a semiconductor layer. As clearly described

in part 2 of Wen's disclosure, In and Al are used to form the n^+ layers which are employed as ohmic contacts for the i-ZnSe layer and for an electrode (i.e., p-type Si layer) formed on the n+ layers, respectively. Thus, interpreting the i-ZnSe layer as a semiconductor layer, Wen clearly does not disclose or describe a plurality of semiconductor layers of a second conductivity type disposed in spaced-apart relation in a surface of the semiconductor substrate, as required by independent claim 15. In Wen, the i-ZnSe layer is a single layer, not a plurality of layers which are disposed in spaced-apart relation. Furthermore, the i-ZnSe layer is formed on the P-Si substrate by vapor phase epitaxy and, therefore, is not disposed in a surface of the P-Si substrate.

Thus, contrary to the Examiner's contention, one of ordinary skill in the art would recognize that the n-type ZnSe layer, not the two n^+ layers, in Wen corresponds to the semiconductor layers recited in independent claim 15. The n-type ZnSe layer in Wen does not comprise a plurality of semiconductor layers formed in spaced-apart relation in a surface of the semiconductor substrate, as required by independent claim 15.

Moreover, even if the foregoing Examiner's interpretations of Wen's PIN photodiode with respect to limitations (1) and (2) of independent claim 15 are adopted,

the resulting structure of Wen's PIN photodiode does not meet the structural limitations of the photodiode recited in independent claim 15. More specifically, in Wen the n^+ layers, which the Examiner interprets as corresponding to the semiconductor layers of claim 15, are formed on the i-ZnSe absorption layer, which the Examiner interprets as corresponding to the semiconductor substrate together with the P-Si substrate. In contrast, independent claim 15 requires that the semiconductor layers are formed in the semiconductor substrate. Thus, even the Examiner's interpretation of Wen's PIN photodiode does not lead to the structure of the photodiode recited in independent claim 15.

With respect to limitation (3), the Examiner contends that Wen discloses a PIN photodiode in which an interface level region of the surface of a semiconductor substrate does not exist between semiconductor layers. Applicant respectfully disagrees with the Examiner's contention and with the Examiner's interpretation of Wen.

As set forth above for limitations (1) and (2), Wen does not disclose or describe a plurality of semiconductor layers disposed in spaced-apart relation in a surface of the semiconductor substrate, as recited in independent claim 15. Accordingly, Wen does not disclose or describe that an interface level region of the surface of the semiconductor

substrate does not exist between the semiconductor layers, as required by independent claim 15. Contrary to the Examiner's contention, one of ordinary skill in the art would recognize that the n-type ZnSe layer, not the two n^+ layers, in Wen corresponds to the semiconductor layers recited in independent claim 15. The n-type ZnSe layer in Wen does not comprise a plurality of semiconductor layers formed in spaced-apart relation in a surface of the semiconductor substrate, as required by independent claim 15. Since the n-type ZnSe layer in Wen does not have the specific structure of the semiconductor layers recited in independent claim 15, Wen clearly does not disclose or describe that an interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers, as required by independent claim 15.

With respect to the Examiner's arguments in the paragraph bridging pages 6-7 of the final Office Action, the etched portion between the n^+ layers in Wen does not correspond to a non-existent interface level region of the surface of the semiconductor substrate between semiconductor layers, as required by independent claim 15. Applicant respectfully submits that the etched portion (i.e., portion denoted by Y in Exhibit B) of the n^+ layers in Wen is for the purpose of forming an electrode pattern and removing a light

obstacle. Nevertheless, even if in Wen the i-ZnSe layer is interpreted to form part of the semiconductor substrate and the n^+ layers are interpreted to correspond to the semiconductor layers, as proposed by the Examiner, there is no disclosure in Wen that an interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers, as required by independent claim 15.

Moreover, the Examiner acknowledges that Wen does not specifically teach the non-existence of an interface level region of the surface of the semiconductor substrate in an area between two semiconductor layers (Final Office Action, pg. 6, lines 9-11). The Examiner contends, however, that Wen follows "exactly the same procedure" (e.g., wet etching) as described in the specification of the present invention in order to achieve the removal of the interface level region of the semiconductor substrate between the semiconductor layers. The Examiner therefore concludes that "the non-existence of an interface level region of the surface of the semiconductor substrate between the semiconductor layers" is "inherent in the device as specified by" Wen. Applicant vigorously disagrees with this contention and with the Examiner's assertion of inherency to support this contention.

The Examiner's assertion that the feature "an interface level region of the surface of the semiconductor

substrate does not exist between the semiconductor layers" in claim 15 is "inherent" in Wen is misplaced because such feature is not necessarily present in Wen as discussed above. As stated by the Federal Circuit in Continental Can Co. USA v. Monsanto Co., 20 USPQ2d 1746, 1749-50 (Fed. Cir. 1991):

> To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference and that it would be so recognized by persons of ordinary skill.

As recognized by the Examiner, Wen discloses the use of standard photolithography and wet etching techniques to implement the PIN photodiode. However, contrary to the Examiner's contention, such techniques are used to remove a portion in the area immediately above the n-type ZnSe layer (note the area denoted by arrow Y in Exhibit B) corresponding to the n+ layers, not the semiconductor layers (i.e., the n-type ZnSe layer in Wen). Thus the feature "an interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers" recited in claim 15 is not present in Wen, and one of ordinary skill in the art would not recognize such feature to be present.

Since Wen does not disclose or describe the foregoing features in independent claim 15, there can be no anticipation by Wen of independent claim 15 under 35 U.S.C. §102(b). That is, since each and every limitation of independent claim 15 is not found in Wen, the reference does not anticipate the claimed invention. See In re Lange, 209 USPQ 288, 293 (CCPA 1981). Furthermore, Wen does not suggest the claimed subject matter and, therefore, would not have motivated one skilled in the art to modify Wen's PIN photodiode to arrive at the claimed invention.

Claim 16 depends on and contains all of the limitations of independent claim 15 and, therefore, distinguishes from the reference at least in the same manner as claim 15.

Moreover, there is a separate ground for patentability of dependent claim 16. Independent claim 15, from which claim 16 depends, requires that the semiconductor substrate is of a first conductivity type and that the semiconductor layers are of a second conductivity type. Claim 16 includes the additional limitation that the first conductivity type is different from the second conductivity type (i.e., the conductivity types of the semiconductor substrate and the semiconductor layers are different). Thus, even if the Examiner's interpretations of Wen's PIN photodiode are adopted with respect to the P-Si substrate and the i-ZnSe

layer together corresponding to the semiconductor substrate of claim 15 and the n^+ layers corresponding to the semiconductor layers recited in claim 15, the resulting structure of Wen's PIN photodiode does not anticipate the structural combination of the photodiode required by dependent claim 16. More specifically, adopting the Examiner's interpretation of Wen, the n-type semiconductor layers (n^+ layers) are disposed on the i-ZnSe absorption layer which of the same type (i.e., n-type) as the semiconductor layers. Thus, even interpreted as proposed by the Examiner, the resulting structure of Wen's PIN photodiode would not result in a photodiode having semiconductor layers of a first conductivity type disposed in a semiconductor substrate of a second conductivity type different from the first conductivity type.
limitations of the photodiode recited in dependent claim 1.

In view of the foregoing, applicant respectfully requests that the rejection of claims 15-16 under 35 U.S.C. §102(b) as being anticipated by Wen be withdrawn.

Rejection Under 35 U.S.C. §103(a)

Claims 1 and 3-7[2] were rejected under 35 U.S.C.

[2] While the Examiner included claim 2 in this ground of rejection, it is clear from pages 4-5 and 10-11 of the final Office Action that the Examiner has withdrawn the rejection of claim 2 under 35 U.S.C. §103(a) as being unpatentable over Wen in view of APD and has rejected claim 2 under 35 U.S.C. §103(a) as being unpatentable over Wen in view of APD and further in view of Chang Son Yin.

§103(a) as being unpatentable over Wen in view of APD. Applicant respectfully traverses this rejection and submits that the combined teachings of Wen and APD do not disclose or suggest the subject matter recited in independent claim 1 and dependent claims 2-7.

Independent claim 1 is directed to a photodiode and requires an optical detection portion for detecting an optical signal and outputting a photoelectric conversion signal, the optical detection portion having a semiconductor substrate of a first conductive type, a plurality of semiconductor layers of a second conductive type formed in spaced-apart relation in a surface of the semiconductor substrate, and a depletion layer formed in the semiconductor substrate by application of a reverse bias to the photodiode so as to surround the semiconductor layers. Independent claim 1 further requires that the depletion layer has an etched surface portion disposed between the semiconductor layers so that an interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers. No corresponding structural combination is disclosed or suggested by the prior art of record.

The primary reference to Wen discloses a PIN photodiode as set forth above for the rejection of claims 15-16 under 35 U.S.C. §102(b). In the statement of rejection,

the Examiner contends that the P-Si substrate and the n-type ZnSe layer in Wen correspond to the semiconductor substrate in independent claim 1 and that the n^+ layers (i.e., ohmic contacts) correspond to the semiconductor layers in independent claim 1. The Examiner further contends that a boundary between the portion of the n^+ layers that has been etched away and the n-type ZnSe layer corresponds to the etched surface portion recited in independent claim 1. Applicant respectfully disagrees with the Examiner's contentions and with the Examiner's interpretation of Wen in the rejection of the claims.

Contrary to the Examiner's contention, one of ordinary skill in the art would recognize that only the P-Si substrate in Wen corresponds to the semiconductor substrate recited in independent claim 1. As described in parts 1-2 of Wen, the absorption layer i-ZnSe in Wen is a heteroepitaxial ZnSe thin film formed on the P-Si substrate by vapor phase epitaxy. After finishing the epitaxial growth, the n^+ -ZnSe layer was achieved by driving evaporated In metal into the ZnSe layer. A P-N junction is thus formed at an interface between the P-Si substrate and the i-ZnSe layer in Wen. Accordingly, contrary to the Examiner's contention, it is evident from the disclosure in Wen that the i-ZnSe layer is a separate layer which cannot be reasonably interpreted as

forming a semiconductor substrate together with the P-Si substrate. Stated otherwise, only the P-Si substrate in Wen can be reasonable interpreted as the semiconductor substrate recited in independent claim 15.

Moreover, Wen does not disclose or describe a plurality of semiconductor layers formed in spaced-apart relation in a surface of the semiconductor substrate, as recited in independent claim 1, as set forth above for the rejection of claims 15-16 under 35 U.S.C. §102(b). Contrary to the Examiner's contention, one of ordinary skill in the art would recognize that the n-type ZnSe layer, not the two n+ layers, in Wen corresponds to the semiconductor layers recited in independent claim 1. The n-type ZnSe layer in Wen does not comprise a plurality of semiconductor layers formed in spaced-apart relation in a surface of the semiconductor substrate, as required by independent claim 1.

Wen also does not disclose or suggest a depletion layer having an etched surface portion disposed between the semiconductor layers so that an interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers, as required by independent claim 1. While acknowledging that neither Wen nor APD specifically teaches this structural feature recited in independent claim 1 (Final Office Action, pg. 9, lines 10-12), the Examiner

contends that this feature "follows from the device specification" of Wen because Wen follows "exactly the same procedure" (e.g., wet etching) as described in the specification of the present invention to achieve the removal of the interface level region of the semiconductor substrate between the semiconductor layers. Applicant vigorously disagrees with the Examiner's contention.

As recognized by the Examiner, Wen discloses the use of standard photolithography and wet etching techniques to implement the PIN photodiode. However, contrary to the Examiner's contention, such techniques are used to remove a portion in the area immediately above the n-type ZnSe layer (note the area denoted by arrow Y in Exhibit B) corresponding to the n^+ layers, not the depletion layer. Stated otherwise, the etched surface portion in Wen corresponds to the n^+ layers, not the depletion layer in the n-type ZnSe layer in Wen. Thus, the depletion layer in Wen clearly does not have an etched surface portion and, more specifically, an etched surface portion disposed between semiconductor layers formed in spaced-apart relation in a surface of a semiconductor substrate, and that an interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers, as required by independent claim 1.

Moreover, even if the structure of the PIN photodiode disclosed by Wen is interpreted in the manner proposed by the Examiner, applicant respectfully submits that the resulting structure does not meet the limitations required by independent claim 1. More specifically, independent claim 1 requires that the depletion layer has an etched surface portion disposed between the semiconductor layers so that an interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers. While Wen discloses that the n^+ layers have an etched surface portion, as discussed above, there is no disclosure or suggestion that the exposed surface of the n-type ZnSe layer (corresponding to the surface of the semiconductor substrate of independent claim 1 in accordance with the Examiner's interpretation) has been etched away. Thus, even by the Examiner's interpretation, the resulting structure of Wen would at best correspond to the structure of the conventional photodiode shown in APD (Fig. 3), where the interface level region of the semiconductor substrate has not been removed.

Moreover, as recognized by the Examiner, Wen does not disclose or suggest a depletion layer formed in the semiconductor substrate by application of a reverse bias to the photodiode so as to surround the semiconductor layers, as recited in independent claim 1. With respect to this feature,

the Examiner cited APD for its disclosure of a photodiode having a depletion layer surrounding semiconductor layers. The Examiner contends that it would have been obvious to one of ordinary skill in the art to modify Wen's photodiode to incorporate this structural feature taught by APD in order to further the purpose of Wen in increasing the sensitivity of the phototiode. Applicant respectfully disagrees with the Examiner's contention.

It is unclear how the Examiner proposes to modify Wen in view of APD so that the depletion layer surrounds the semiconductor layers in Wen as interpreted by the Examiner (i.e., the n^+ layers). Nevertheless, as discussed above, one of ordinary skill in the art would recognize the n-type ZnSe layer, not the n^+ layers, as corresponding to the semiconductor layers in Wen. There is nothing in the references that would expressly or implicitly teach or suggest the modification urged by the Examiner and, therefore, the references do not directly establish this obviousness.

Thus one of ordinary skill in the art would not have been led to modify Wen in view of APD in the manner proposed by the Examiner in the statement of rejection. The only basis for the modifications urged by the Examiner in the rejection is applicant's own disclosure, and such hindsighted rejections are improper. See, for example, Diversitech Corp. v. Century

Steps, Inc., 7 USPQ2d 1315, 1318 (Fed. Cir. 1988); In re Geiger, 2 USPQ2d 1276, 1278 (Fed. Cir. 1987); Panduit Corp. v. Dennison Manufacturing Co., 227 USPQ 337, 343 (Fed. Cir. 1985); Interconnect Planning Corp. v. Feil, 227 USPQ 543, 551 (Fed. Cir. 1985).

Claims 3-7 depend on and contain all of the limitations of independent claim 1 and, therefore, distinguish from the references at least in the same manner as claim 1.

In view of the foregoing, applicant respectfully requests that the rejection of claim 1 and 3-7 under 35 U.S.C. §103(a) as being unpatentable over Wen in view of APD be withdrawn.

Claim 2 was rejected under 35 U.S.C. §103(a) as being unpatentable over Wen in view of APD and further in view of Chang Song Yin. Applicant respectfully traverses this rejection and submits that the combined teachings of Wen, APD and Chang Song Yin do not disclose or suggest the subject matter recited in independent claim 2.

Wen in view of APD does not disclose or suggest the subject matter recited in independent claim 1 as set forth above for the rejection of claims 1 and 3-7 under 35 U.S.C. §103(a) as being unpatentable over Wen in view of APD. Claim 2 depends on and contains all of the limitations of independent claim 1 and, therefore, distinguishes from the references at least in the same manner as claim 1.

The secondary reference to Chang Song Yin has been cited by the Examiner for its disclosure of a photodiode in which the ratio of the distance between semiconductor layers and a width of a depletion layer falls within the range recited in claim 2. However, Chang Song Yin clearly does not disclose or suggest the structural combination of the semiconductor substrate, depletion layer and semiconductor layers, including the non-existence of the interface level region of the surface of the semiconductor substrate, as recited in independent claim 1, from which claim 2 depends. Since Chang Song Yin does not disclose or suggest the foregoing structural combination of independent claim 1, it does not cure the deficiencies of Wen as modified by APD. Accordingly, one of ordinary skill in the art would not have been led to modify the references to attain the claimed subject matter.

In view of the foregoing, applicant respectfully requests that the rejection of claim 2 under 35 U.S.C. §103(a) as being unpatentable over Wen in view of APD and further in view of Chang Song Yin be withdrawn.

In view of the foregoing amendments and discussion, the application is believed to be in allowable form. Accordingly, favorable reconsideration and allowance of the claims are most respectfully requested.

Respectfully submitted,

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MAILING CERTIFICATE

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Signature

November 28, 2003
Date

EXHIBIT A

FIG. 1

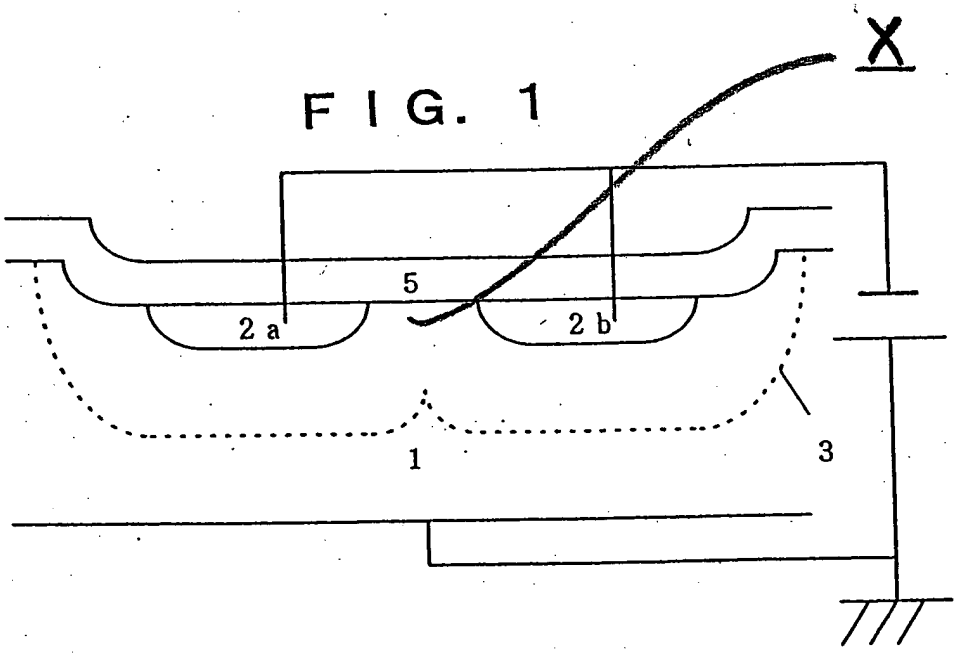

EXHIBIT B